

IN THE SPECIFICATION:

Please amend the paragraph beginning at page 8 line 10 as follows:

As shown in the following figures, in a conventional Field Effect  
5 ~~Transformer~~ Transistor (FET) setting, a gated diode can be formed by the source and the  
gate of a three terminal FET device (either n-type or p-type), with the drain floating (e.g.,  
disconnected or nonexistent), as shown in (for example) FIGS. 1B, 4B, 6 and 8.  
Sometimes the source and drain of such a FET can be connected together at the same  
potential ~~an~~ and may be viewed as two gated diodes connected in parallel, as shown in  
10 (for example) FIGS 2B, 5B, 7 and 9. In this disclosure, these two situations are used  
interchangeably. And without specifying explicitly, a gated diode is referred to just the  
first basic form, only a source and a gate of a semiconductor device.

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